FTU=s, T=3*FTU, B=2, S=12, FTU=120 Picosecond Modulation Example

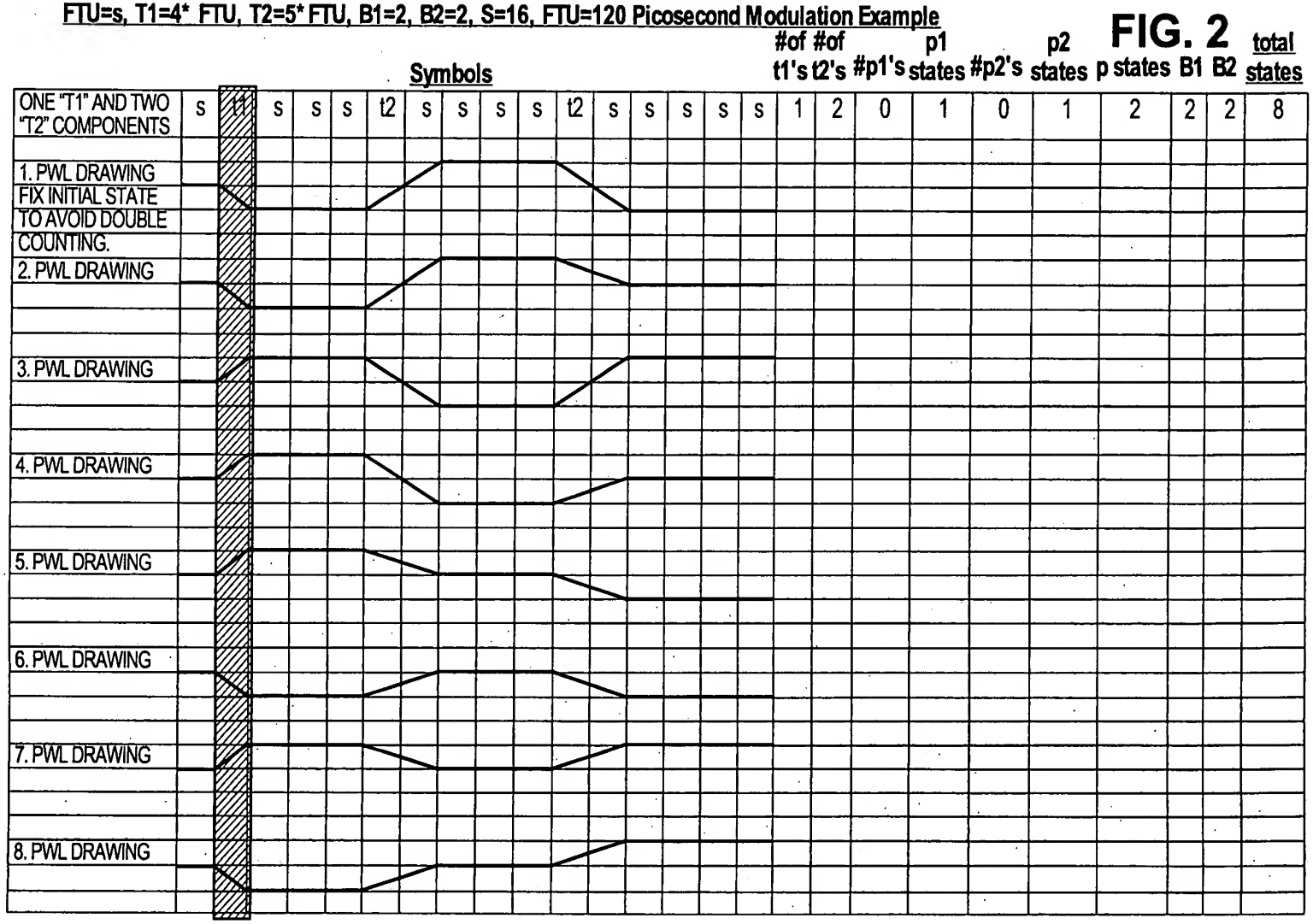
# edges	Symbols												# of t's	# of p's	# p states	total states	Comments
~~0 edge~~	~~s~~	~~s~~	~~s~~	~~s~~	~~s~~	~~s~~	~~s~~	~~s~~	~~s~~	~~s~~	~~s~~	~~s~~	~~0~~	~~0~~	~~1~~	~~1~~	Don't use this state
1 edge	p	p	p	p	p	p	p	p	p	t	s	s	1	9	10	20	
2 edge	t	s	s	p	p	p	p	p	p	t	s	s	2	6	7	28	
2 edge	s	t	s	s	p	p	p	p	p	t	s	s	2	5	6	24	
2 edge	s	s	t	s	s	p	p	p	p	t	s	s	2	4	5	20	
2 edge	s	s	s	t	s	s	p	p	p	t	s	s	2	3	4	16	
2 edge	s	s	s	s	t	s	s	p	p	t	s	s	2	2	3	12	
2 edge	s	s	s	s	s	t	s	s	p	t	s	s	2	1	2	8	
2 edge	s	s	s	s	s	s	t	s	s	t	s	s	2	0	1	4	
3 edge	t	s	s	t	s	s	p	p	p	t	s	s	3	3	4	32	
3 edge	t	s	s	s	t	s	s	p	p	t	s	s	3	2	3	24	
3 edge	t	s	s	s	s	t	s	s	p	t	s	s	3	1	2	16	
3 edge	t	s	s	s	s	s	t	s	s	t	s	s	3	0	1	8	
3 edge	s	t	s	s	t	s	s	p	p	t	s	s	3	2	3	24	
3 edge	s	t	s	s	s	t	s	s	p	t	s	s	3	1	2	16	
3 edge	s	t	s	s	s	s	t	s	s	t	s	s	3	0	1	8	
3 edge	s	s	t	s	s	t	s	s	p	t	s	s	3	1	2	16	
3 edge	s	s	t	s	s	s	t	s	s	t	s	s	3	0	1	8	
3 edge	s	s	s	t	s	s	t	s	s	t	s	s	3	0	1	8	
4 edge	t	s	s	t	s	s	t	s	s	t	s	s	4	0	1	16	"Binary"
															59	308	

Total p states	59	1 Edge P States	10	**columns**	12
Total States	308	2 Edge P States	28	**frequency**	6.94E+08
Total mod	8.266786541	3 Edge P States	20	**Payload**	5.56E+09
Total trunc mod	8	4 Edge P States	1	**Payload Ratio**	1.33
				Payload Ratio versus "binary"	2.00

FIG. 1

FTU=s, T1=4* FTU, T2=5* FTU, B1=2, B2=2, S=16, FTU=120 Picosecond Modulation Example

FIG. 2



FTU=s, T1=4* FTU, T2=5* FTU, B1=2, B2=2, S=16, FTU=120 Picosecond Modulation Example

FIG. 3

Clock:	t1	s	s	s	t1	s	s	s	t1	s	s	s	t1	s	s	s
Clk Edge#:	1				2				3				4			
Slot#:																
Clock	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Assignment	1	1	1	1	2	2	2	2	3	3	3	3	4	4	4	4

# edges	Symbols	# of t1's	# of t2's	#p1's	p1'states	#p2's	p2'states	p states	B1	B2	total states
1 T1	p1 p1 p1 p1 p1 p1 p1 p1 p1 p1 p1 p1 s s s	1	0	12	13	0	1	14	2	2	26
2 T1	t1 s s s p1 p1 p1 p1 p1 p1 p1 p1 s s s	2	0	8	9	0	1	10	2	2	36
2 T1	s t1 s s s p1 p1 p1 p1 p1 p1 p1 s s s	2	0	7	8	0	1	9	2	2	32
2 T1	s s t1 s s s p1 p1 p1 p1 p1 p1 s s s	2	0	6	7	0	1	8	2	2	28
2 T1	s s s t1 s s s p1 p1 p1 p1 p1 s s s	2	0	5	6	0	1	7	2	2	24
2 T1	s s s s t1 s s s p1 p1 p1 p1 s s s	2	0	4	5	0	1	6	2	2	20
2 T1	s s s s s t1 s s s p1 p1 p1 s s s	2	0	3	4	0	1	5	2	2	16
2 T1	s s s s s s t1 s s s p1 p1 s s s	2	0	2	3	0	1	4	2	2	12
2 T1	s s s s s s s t1 s s s p1 s s s	2	0	1	2	0	1	3	2	2	8
2 T1	s s s s s s s s t1 s s s s s s	2	0	0	1	0	1	2	2	2	4
3 T1	t1 s s s t1 s s s s p1 s p1 s s s	3	0	4	5	0	1	6	2	2	40
3 T1	t1 s s s s t1 s s s s t1 p1 s s s	3	0	3	4	0	1	5	2	2	32
3 T1	t1 s s s s s t1 s s s s p1 s s s	3	0	2	3	0	1	4	2	2	24
3 T1	t1 s s s s s s t1 s s s p1 s s s	3	0	1	2	0	1	3	2	2	16
3 T1	t1 s s s s s s s t1 s s s s s s	3	0	0	1	0	1	2	2	2	8
3 T1	s t1 s s s s s s s p1 p1 p1 s s s	3	0	3	4	0	1	5	2	2	32
3 T1	s t1 s s s s s s s s p1 p1 s s s	3	0	2	3	0	1	4	2	2	24
3 T1	s t1 s s s s s s s s s p1 s s s	3	0	1	2	0	1	3	2	2	16
3 T1	s t1 s s s s s s s s s s s s s	3	0	0	1	0	1	2	2	2	8
3 T1	s s t1 s s s s s s s p1 p1 s s s	3	0	2	3	0	1	4	2	2	24
3 T1	s s t1 s s s s s s s s p1 s s s	3	0	1	2	0	1	3	2	2	16
3 T1	s s t1 s s s s s s s s s s s s	3	0	0	1	0	1	2	2	2	8
3 T1	s s s t1 s s s s s s s p1 s s s	3	0	1	2	0	1	3	2	2	16
3 T1	s s s t1 s s s s s s s s s s s	3	0	0	1	0	1	2	2	2	8
3 T1	s s s s t1 s s s s s s s s s s	3	0	0	1	0	1	2	2	2	8

4	T1	t1	s	s	s	t1	s	s	s	t1	s	s	s	t1	s	s	s	4	0	0	1	0	1	2	2	2	16
1	T2	p2	p2	p2	p2	p2	p2	p2	p2	p2	p2	p2	t2	s	s	s	s	0	1	0	1	11	12	13	2	2	24
2	T2	t2	s	s	s	s	p2	p2	p2	p2	p2	p2	t2	s	s	s	s	0	2	0	1	6	7	8	2	2	28
2	T2	s	t2	s	s	s	s	p2	p2	p2	p2	p2	t2	s	s	s	s	0	2	0	1	5	6	7	2	2	24
2	T2	s	s	t2	s	s	s	s	p2	p2	p2	p2	t2	s	s	s	s	0	2	0	1	4	5	6	2	2	20
2	T2	s	s	s	t2	s	s	s	s	p2	p2	p2	t2	s	s	s	s	0	2	0	1	3	4	5	2	2	16
2	T2	s	s	s	s	t2	s	s	s	s	p2	p2	t2	s	s	s	s	0	2	0	1	2	3	4	2	2	12
2	T2	s	s	s	s	s	t2	s	s	s	s	p2	t2	s	s	s	s	0	2	0	1	1	2	3	2	2	8
2	T2	s	s	s	s	s	s	t2	s	s	s	s	t2	s	s	s	s	0	2	0	1	0	1	2	2	2	4
3	T2	t2	s	s	s	s	ts	s	s	s	s	p2	t2	s	s	s	s	0	3	0	1	1	2	3	2	2	16
3	T2	t2	s	s	s	s	s	t2	s	s	s	s	t2	s	s	s	s	0	3	0	1	0	1	2	2	2	8
3	T2	s	t2	s	s	s	s	t2	s	s	s	s	t2	s	s	s	s	0	3	0	1	0	1	2	2	2	8
T2	T1	t2	s	s	s	s	p1	p1	p1	p1	p1	p1	p1	t1	s	s	s	1	1	7	8	0	1	9	2	2	23
T2	T1	s	t2	s	s	s	s	p1	p1	p1	p1	p1	p1	t1	s	s	s	1	1	6	7	0	1	8	2	2	28
T2	T1	s	s	t2	s	s	s	s	p1	p1	p1	p1	p1	t1	s	s	s	1	1	5	6	0	1	7	2	2	24
T2	T1	s	s	s	t2	s	s	s	s	p1	p1	p1	p1	t1	s	s	s	1	1	4	5	0	1	6	2	2	20
T2	T1	s	s	s	s	t2	s	s	s	s	p1	p1	p1	t1	s	s	s	1	1	3	4	0	1	5	2	2	16
T2	T1	s	s	s	s	s	t2	s	s	s	s	p1	p1	t1	s	s	s	1	1	2	3	0	1	4	2	2	12
T2	T1	s	s	s	s	s	s	t2	s	s	s	s	p1	t1	s	s	s	1	1	1	2	0	1	3	2	2	8
T2	T1	s	s	s	s	s	s	s	t2	s	s	s	s	t1	s	s	s	1	1	0	1	0	1	2	2	2	4
T1	T2	t1	s	s	s	p2	p2	p2	p2	p2	p2	p2	t2	s	s	s	s	1	1	0	1	7	8	9	2	2	32
T1	T2	s	t1	s	s	s	p2	p2	p2	p2	p2	p2	t2	s	s	s	s	1	1	0	1	6	7	8	2	2	28
T1	T2	s	s	t1	s	s	s	p2	p2	p2	p2	p2	t2	s	s	s	s	1	1	0	1	5	6	7	2	2	24
T1	T2	s	s	s	t1	s	s	s	p2	p2	p2	p2	t2	s	s	s	s	1	1	0	1	4	5	6	2	2	20
T1	T2	s	s	s	s	t1	s	s	s	p2	p2	p2	t2	s	s	s	s	1	1	0	1	3	4	5	2	2	16

FIG. 3 (cont.)

T1 T2		s	s	s	s	s	t1	s	s	s	p2	p2	t2	s	s	s	s	1	1	0	1	2	3	4	2	2	12
T1 T2		s	s	s	s	s	s	t1	s	s	s	p2	t2	s	s	s	s	1	1	0	1	1	2	3	2	2	8
T1 T2		s	s	s	s	s	s	s	t1	s	s	s	t2	s	s	s	s	1	1	0	1	0	1	2	2	2	4
T1 T2 T2	t1	s	s	s	s	s	s	s	s	p2	p2	t2	s	s	s	s		1	2	0	1	2	3	4	2	2	24
T1 T2 T2	t1	s	s	s	s	t2	s	s	s	s	p2	t2	s	s	s	s		1	2	0	1	1	2	3	2	2	16
T1 T2 T2	t1	s	s	s	s	s	t2	s	s	s	s	t2	s	s	s	s		1	2	0	1	0	1	2	2	2	8
T1 T2 T2	s	t1	s	s	s	t2	s	s	s	s	p2	t2	s	s	s	s		1	2	0	1	1	2	3	2	2	16
T1 T2 T2	s	t1	s	s	s	s	t2	s	s	s	s	t2	s	s	s	s		1	2	0	1	0	1	2	2	2	8
T1 T2 T2	s	s	t1	s	s	s	t2	s	s	s	s	t2	s	s	s	s		1	2	0	1	0	1	2	2	2	8
T2 T1 T2	t2	s	s	s	s	t1	s	s	s	p2	p2	t2	s	s	s	s		1	2	0	1	2	3	4	2	2	24
T2 T1 T2	t2	s	s	s	s	s	t1	s	s	s	p2	t2	s	s	s	s		1	2	0	1	1	2	3	2	2	16
T2 T1 T2	t2	s	s	s	s	s	s	t1	s	s	s	t2	s	s	s	s		1	2	0	1	0	1	2	2	2	8
T2 T1 T2	s	t2	s	s	s	s	t1	s	s	s	p2	t2	s	s	s	s		1	2	0	1	1	2	3	2	2	16
T2 T1 T2	s	t2	s	s	s	s	s	t1	s	s	s	t2	s	s	s	s		1	2	0	1	0	1	2	2	2	8
T2 T1 T2	s	s	t2	s	s	s	s	t1	s	s	s	t2	s	s	s	s		1	2	0	1	0	1	2	2	2	8
T2 T2 T1	t2	s	s	s	s	t2	s	s	s	s	p1	p1	t1	s	s	s		1	2	2	3	0	1	4	2	2	24
T2 T2 T1	t2	s	s	s	s	s	t2	s	s	s	s	p1	t1	s	s	s		1	2	1	2	0	1	3	2	2	16
T2 T2 T1	t2	s	s	s	s	s	s	t2	s	s	s	s	t1	s	s	s		1	2	0	1	0	1	2	2	2	8
T2 T2 T1	s	t2	s	s	s	s	t2	s	s	s	s	p1	t1	s	s	s		1	2	1	2	0	1	3	2	2	16
T2 T2 T1	s	t2	s	s	s	s	s	t2	s	s	s	s	t1	s	s	s		1	2	0	1	0	1	2	2	2	8
T2 T2 T1	s	s	t2	s	s	s	s	t2	s	s	s	s	t1	s	s	s		1	2	0	1	0	1	2	2	2	8
T2 T1 T1	t2	s	s	s	s	t1	s	s	s	p1	p1	p1	t1	s	s	s		2	1	3	4	0	1	5	2	2	32
T2 T1 T1	t2	s	s	s	s	s	t1	s	s	s	p1	p1	t1	s	s	s		2	1	2	3	0	1	4	2	2	24
T2 T1 T1	t2	s	s	s	s	s	s	t1	s	s	s	p1	t1	s	s	s		2	1	1	2	0	1	3	2	2	16
T2 T1 T1	t2	s	s	s	s	s	s	s	t1	s	s	s	t1	s	s	s		2	1	0	1	0	1	2	2	2	8

FIG. 3 (cont.)

T2 T1 T1	s	t2	s	s	s	s	t1	s	s	s	p1	p1	t1	s	s	s	2	1	2	3	0	1	4	2	2	24
T2 T1 T1	s	t2	s	s	s	s	s	t1	s	s	s	p1	t1	s	s	s	2	1	1	2	0	1	3	2	2	16
T2 T1 T1	s	t2	s	s	s	s	s	s	t1	s	s	s	t1	s	s	s	2	1	0	1	0	1	2	2	2	8
T2 T1 T1	s	s	t2	s	s	s	s	t1	s	s	s	p1	t1	s	s	s	2	1	1	2	0	1	3	2	2	16
T2 T1 T1	s	s	t2	s	s	s	s	s	t1	s	s	s	t1	s	s	s	2	1	0	1	0	1	2	2	2	8
T2 T1 T1	s	s	s	t2	s	s	s	s	t1	s	s	s	t1	s	s	s	2	1	0	1	0	1	2	2	2	8
T1 T2 T1	t1	s	s	s	t2	s	s	s	s	p1	p1	p1	t1	s	s	s	2	1	3	4	0	1	5	2	2	32
T1 T2 T1	t1	s	s	s	s	t2	s	s	s	s	p1	p1	t1	s	s	s	2	1	2	3	0	1	4	2	2	24
T1 T2 T1	t1	s	s	s	s	s	t2	s	s	s	s	p1	t1	s	s	s	2	1	1	2	0	1	3	2	2	16
T1 T2 T1	t1	s	s	s	s	s	s	t2	s	s	s	s	t1	s	s	s	2	1	0	1	0	1	2	2	2	8
T1 T2 T1	s	t1	s	s	s	t2	s	s	s	s	p1	p1	t1	s	s	s	2	1	2	3	0	1	4	2	2	24
T1 T2 T1	s	t1	s	s	s	s	t2	s	s	s	s	p1	t1	s	s	s	2	1	1	2	0	1	3	2	2	16
T1 T2 T1	s	t1	s	s	s	s	s	t2	s	s	s	s	t1	s	s	s	2	1	0	1	0	1	2	2	2	8
T1 T2 T1	s	s	t1	s	s	s	t2	s	s	s	s	p1	t1	s	s	s	2	1	1	2	0	1	3	2	2	16
T1 T2 T1	s	s	t1	s	s	s	s	t2	s	s	s	s	t1	s	s	s	2	1	0	1	0	1	2	2	2	8
T1 T2 T1	s	s	s	t1	s	s	s	t2	s	s	s	s	t1	s	s	s	2	1	0	1	0	1	2	2	2	8
T1 T1 T2	t1	s	s	s	t1	s	s	s	p2	p2	p2	t2	s	s	s	s	2	1	0	1	3	4	5	2	2	32
T1 T1 T2	t1	s	s	s	s	t1	s	s	s	p2	p2	t2	s	s	s	s	2	1	0	1	2	3	4	2	2	24
T1 T1 T2	t1	s	s	s	s	s	t1	s	s	s	p2	t2	s	s	s	s	2	1	0	1	1	2	3	2	2	16
T1 T1 T2	t1	s	s	s	s	s	s	t1	s	s	s	t2	s	s	s	s	2	1	0	1	0	1	2	2	2	8
T1 T1 T2	s	t1	s	s	s	t1	s	s	s	p2	p2	t2	s	s	s	s	2	1	0	1	2	3	4	2	2	24
T1 T1 T2	s	t1	s	s	s	s	t1	s	s	s	p2	t2	s	s	s	s	2	1	0	1	1	2	3	2	2	16
T1 T1 T2	s	t1	s	s	s	s	s	t1	s	s	s	t2	s	s	s	s	2	1	0	1	0	1	2	2	2	8
T1 T1 T2	s	s	t1	s	s	s	t1	s	s	s	p2	t2	s	s	s	s	2	1	0	1	1	2	3	2	2	16
T1 T1 T2	s	s	t1	s	s	s	s	t1	s	s	s	t2	s	s	s	s	2	1	0	1	0	1	2	2	2	8
T1 T1 T2	s	s	s	t1	s	s	s	t1	s	s	s	t2	s	s	s	s	2	1	0	1	0	1	2	2	2	8
																				221		180				1678

FIG. 3 (cont.)

Total p states	401
Total States	1678
Total mod	1.0712527000439800E+01
Total trunc mod	10
columns	16
frequency	5.21E+08
Payload	5.58E+09
Payload Ratio	1.34
Payload Ratio (Truncate)	1.2844987615765900E+00

FIG. 3 (cont.)

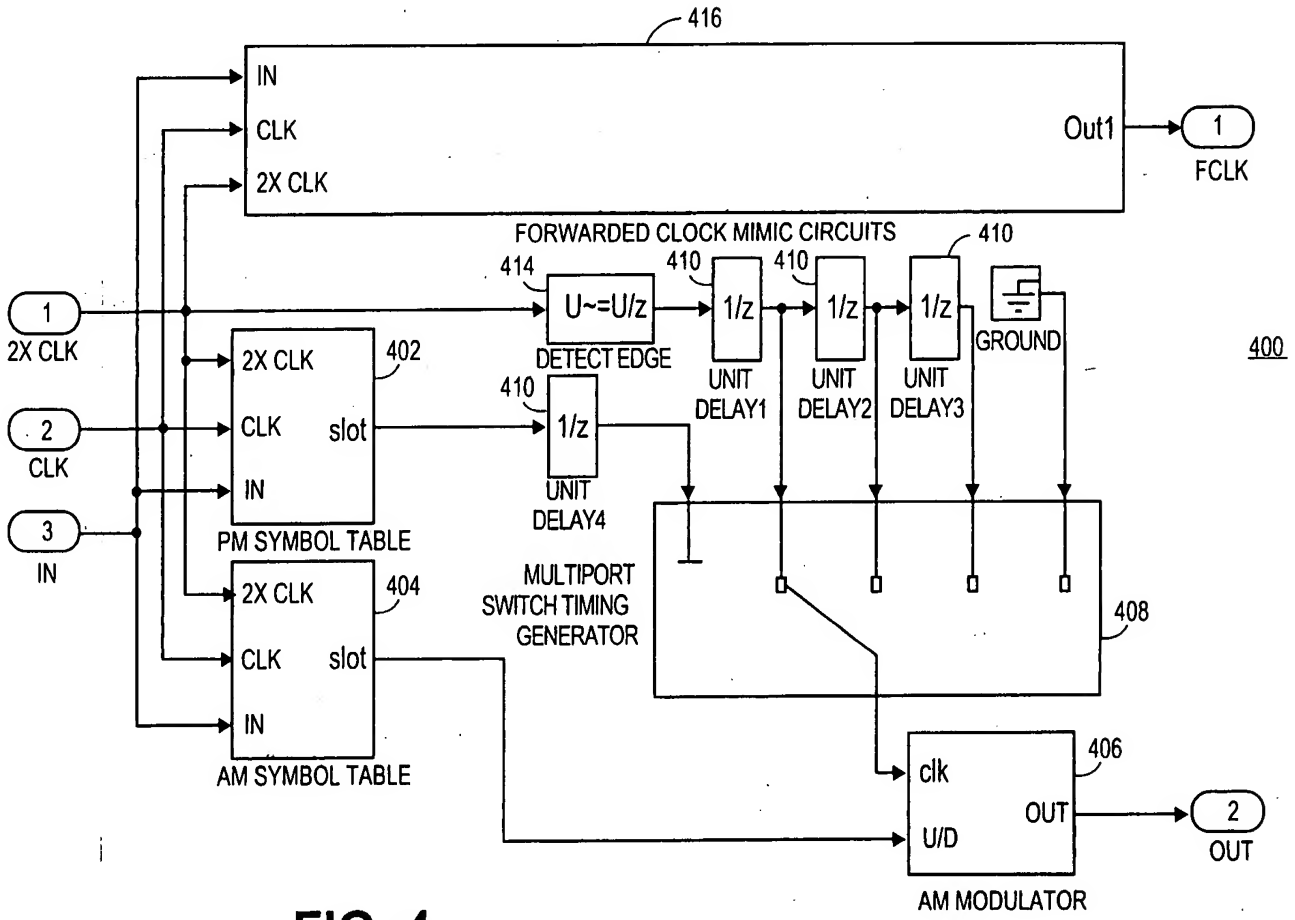

416
IN
CLK
2X CLK
Out1
1
FCLK
FORWARDED CLOCK MIMIC CIRCUITS
410
414
410
410
1
2X CLK
U~=U/z
1/z
1/z
1/z
GROUND
400
DETECT EDGE
UNIT DELAY1
UNIT DELAY2
UNIT DELAY3
2X CLK
402
410
2
CLK
CLK
slot
1/z
IN
UNIT DELAY4
3
IN
PM SYMBOL TABLE
MULTIPORT SWITCH TIMING GENERATOR
2X CLK
404
408
CLK
slot
IN
AM SYMBOL TABLE
clk
406
OUT
2
U/D
OUT
AM MODULATOR

FIG. 4

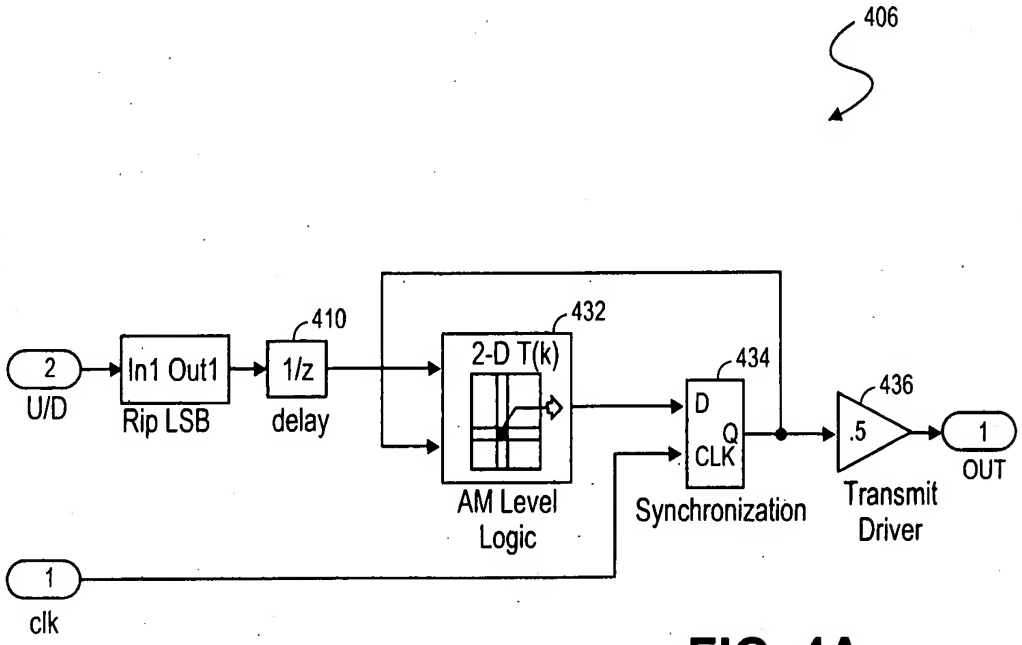

406
2
U/D
In1 Out1
Rip LSB
410
1/z
delay
432
2-D T(k)
AM Level
Logic
434
D
Q
CLK
Synchronization
436
.5
Transmit
Driver
1
OUT
1
clk

FIG. 4A

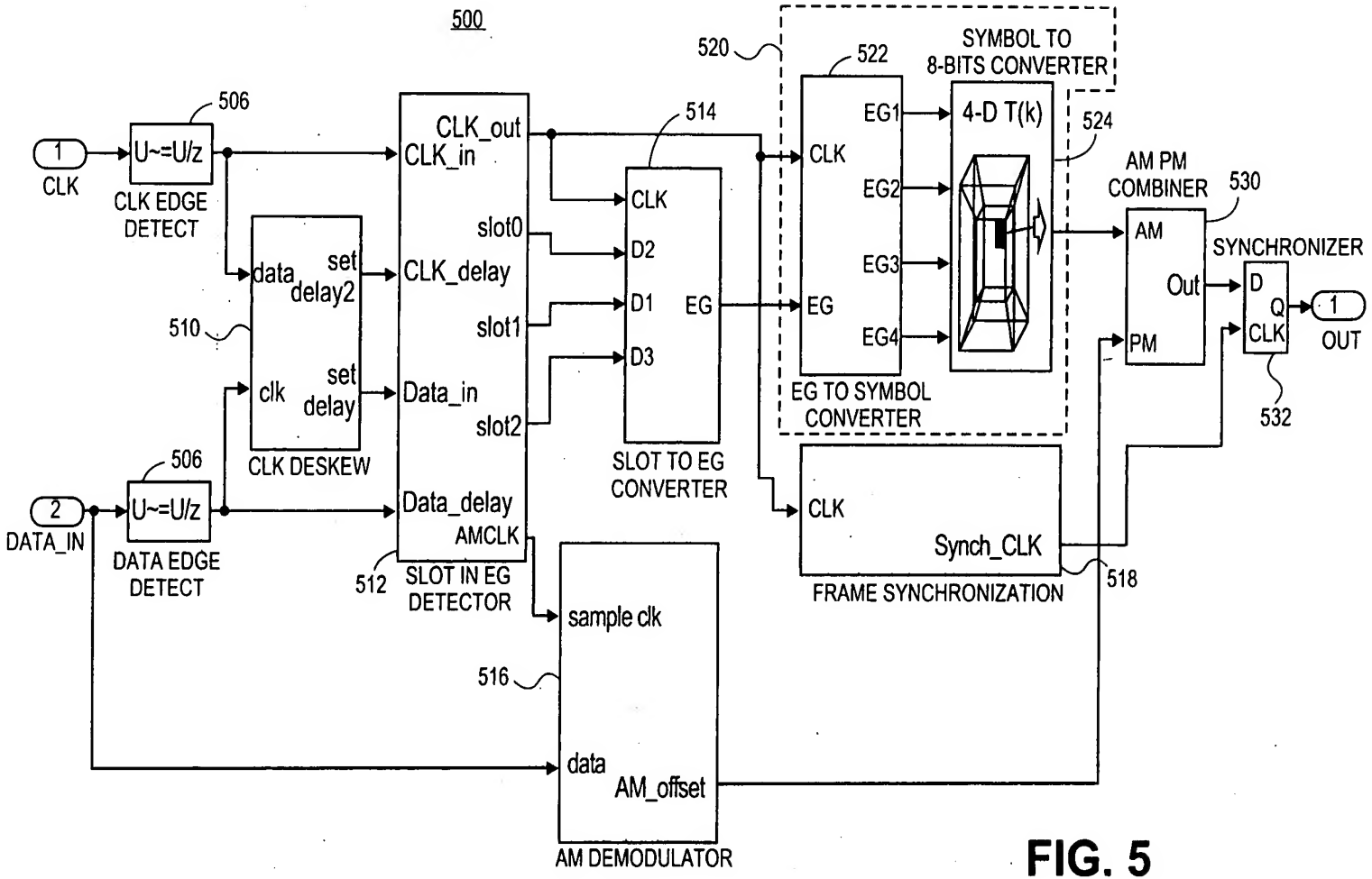

500
1
CLK
U~=U/z
506
CLK EDGE DETECT
data
set delay2
clk
set delay
510
CLK DESKEW
2
DATA_IN
U~=U/z
506
DATA EDGE DETECT
CLK_out
CLK_in
slot0
CLK_delay
slot1
Data_in
slot2
Data_delay
AMCLK
512
SLOT IN EG DETECTOR
514
CLK
D2
D1
EG
D3
SLOT TO EG CONVERTER
520
522
SYMBOL TO 8-BITS CONVERTER
CLK
EG
EG1
EG2
EG3
EG4
4-D T(k)
524
EG TO SYMBOL CONVERTER
AM PM COMBINER
530
AM
Out
PM
SYNCHRONIZER
D
Q
CLK
1
OUT
532
CLK
Synch_CLK
FRAME SYNCHRONIZATION
518
sample clk
516
data
AM_offset
AM DEMODULATOR

FIG. 5

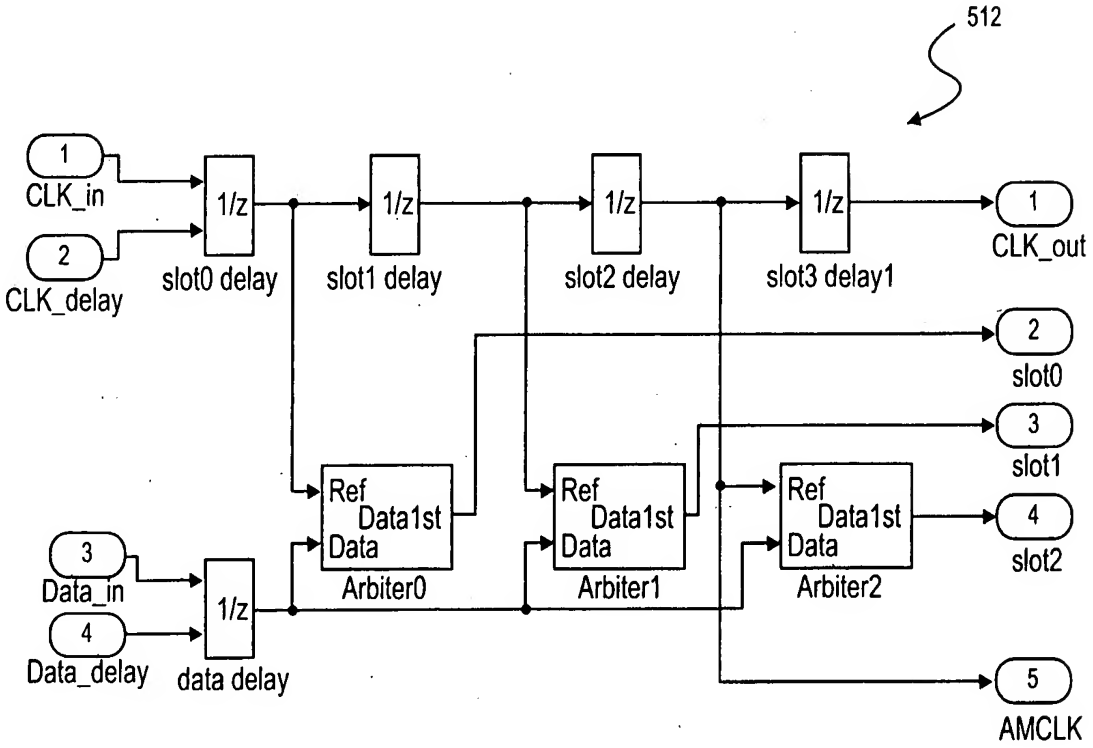

512
1
CLK_in
2
CLK_delay
1/z
slot0 delay
1/z
slot1 delay
1/z
slot2 delay
1/z
slot3 delay1
1
CLK_out
2
slot0
3
slot1
4
slot2
5
AMCLK
Ref
Data1st
Data
Arbiter0
Ref
Data1st
Data
Arbiter1
Ref
Data1st
Data
Arbiter2
3
Data_in
4
Data_delay
1/z
data delay

FIG. 5A

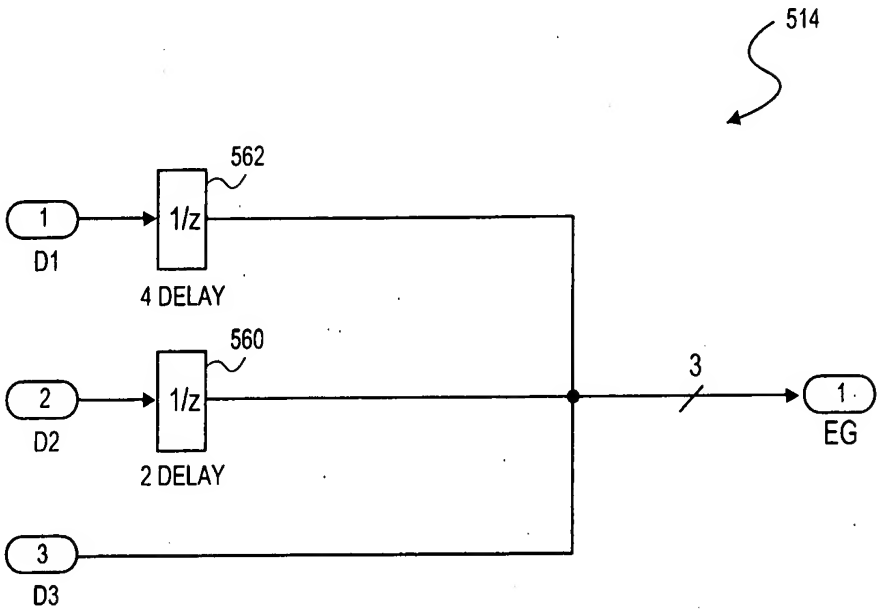


FIG. 5B

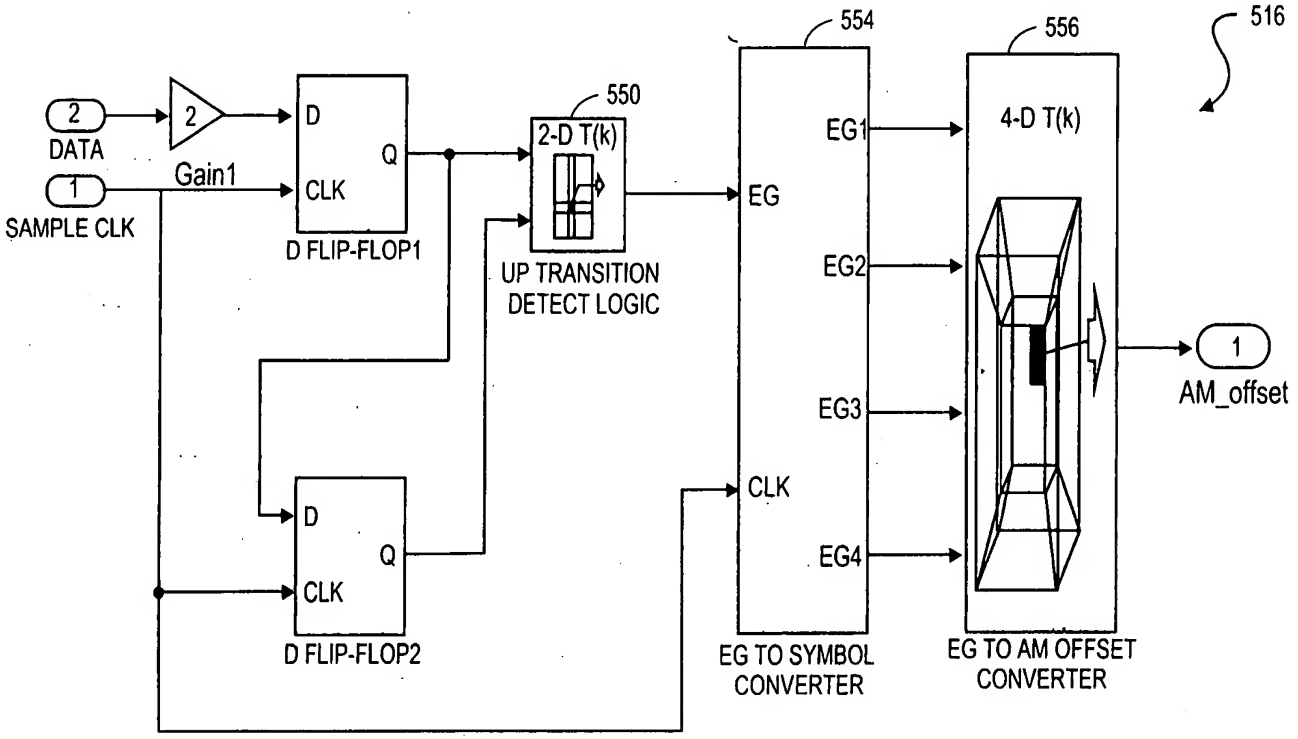

516
554
556
550
2
DATA
1
SAMPLE CLK
2
Gain1
D
CLK
Q
D FLIP-FLOP1
2-D T(k)
UP TRANSITION
DETECT LOGIC
EG
CLK
EG1
EG2
EG3
EG4
EG TO SYMBOL
CONVERTER
4-D T(k)
EG TO AM OFFSET
CONVERTER
1
AM_offset
D
CLK
Q
D FLIP-FLOP2

FIG. 5C

FTU=s,T=3* FTU,B=2,S=12,FTU=120 Picosecond Modulation Example

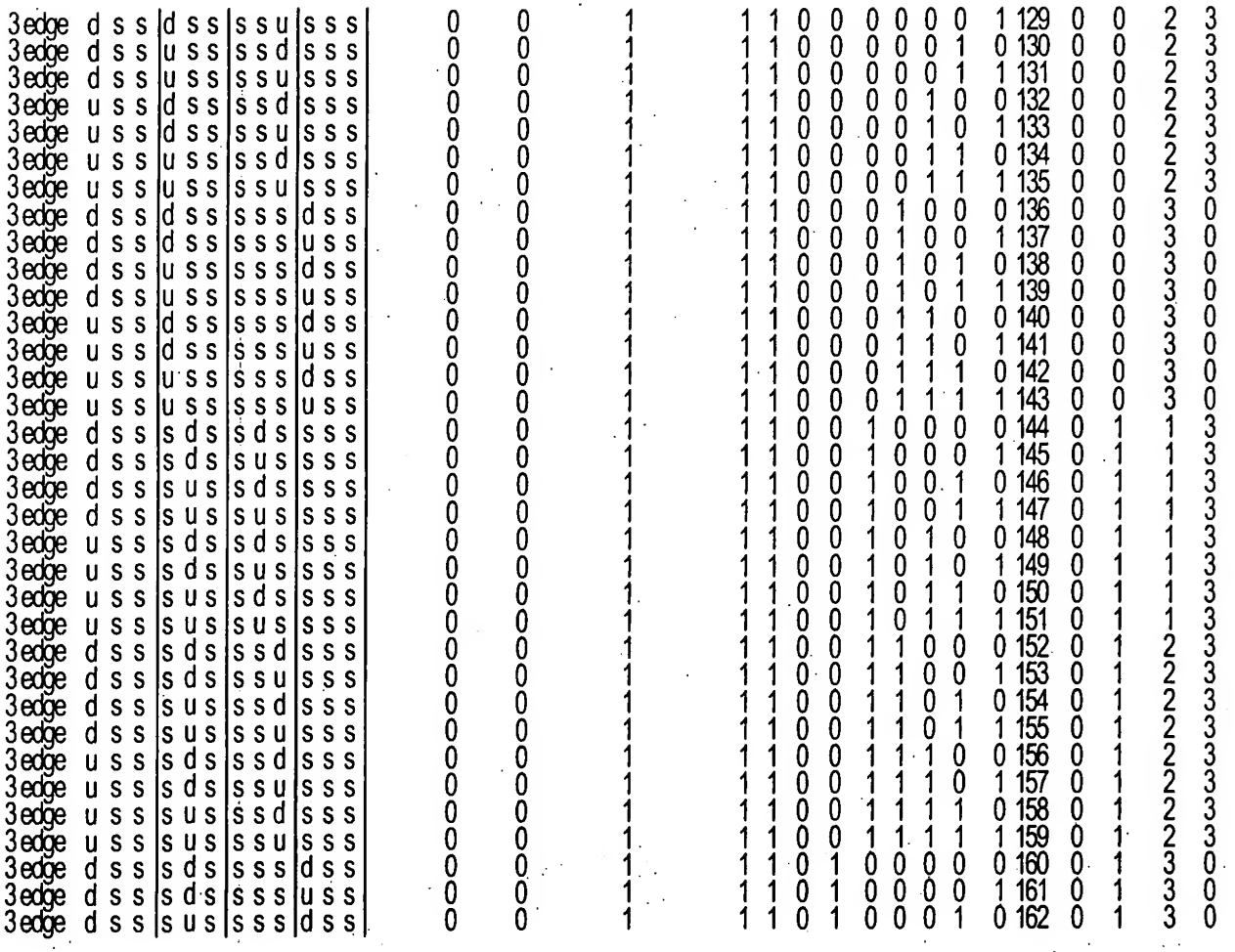
FIG. 6

	Symbols								Mapping to 8 bit modulation								#	Control Signals			
	EG1	EG2	EG3	EG4	# of t's	# of p's	# p states	total states	7	6	5	4	3	2	1	0		EG1	EG2	EG3	EG4
0 edge	s s s	s s s	s s s	s s s	0	0	4	4	Not Used												
1 edge	ŧ s s	s s s	s s s	s s s	4	0	4	2	Not Used												
1 edge	s ŧ s	s s s	s s s	s s s	4	0	4	2	Not Used												
1 edge	s s ŧ	s s s	s s s	s s s	4	0	4	2	Not Used												
1 edge	s s s	ŧ s s	s s s	s s s	4	0	4	2	Not Used												
1 edge	s s s	s d s	s s s	s s s	0	0	1	1	0	0	0	0	0	0	0	0	0	3	1	3	3
1 edge	s s s	s u s	s s s	s s s	0	0	1	1	0	0	0	0	0	0	0	1	1	3	1	3	3
1 edge	s s s	s s d	s s s	s s s	0	0	1	1	0	0	0	0	0	0	1	0	2	3	2	3	3
1 edge	s s s	s s u	s s s	s s s	0	0	1	1	0	0	0	0	0	0	1	1	3	3	2	3	3
1 edge	s s s	s s s	d s s	s s s	0	0	1	1	0	0	0	0	0	1	0	0	4	3	3	0	3
1 edge	s s s	s s s	u s s	s s s	0	0	1	1	0	0	0	0	0	1	0	1	5	3	3	0	3
1 edge	s s s	s s s	s d s	s s s	0	0	1	1	0	0	0	0	0	1	1	0	6	3	3	1	3
1 edge	s s s	s s s	s u s	s s s	0	0	1	1	0	0	0	0	0	1	1	1	7	3	3	1	3
1 edge	s s s	s s s	s s d	s s s	0	0	1	1	0	0	0	0	1	0	0	0	8	3	3	2	3
1 edge	s s s	s s s	s s u	s s s	0	0	1	1	0	0	0	0	1	0	0	1	9	3	3	2	3
1 edge	s s s	s s s	s s s	d s s	0	0	1	1	0	0	0	0	1	0	1	0	10	3	3	3	0
1 edge	s s s	s s s	s s s	u s s	0	0	1	1	0	0	0	0	1	0	1	1	11	3	3	3	0
2 edge	d s s	d s s	s s s	s s s	0	0	1	1	0	0	0	0	1	1	0	0	12	0	0	3	3
2 edge	d s s	u s s	s s s	s s s	0	0	1	1	0	0	0	0	1	1	0	1	13	0	0	3	3
2 edge	u s s	d s s	s s s	s s s	0	0	1	1	0	0	0	0	1	1	1	0	14	0	0	3	3
2 edge	u s s	u s s	s s s	s s s	0	0	1	1	0	0	0	0	1	1	1	1	15	0	0	3	3
2 edge	d s s	s d s	s s s	s s s	0	0	1	1	0	0	0	1	0	0	0	0	16	0	1	3	3
2 edge	d s s	s u s	s s s	s s s	0	0	1	1	0	0	0	1	0	0	0	1	17	0	1	3	3
2 edge	u s s	s d s	s s s	s s s	0	0	1	1	0	0	0	1	0	0	1	0	18	0	1	3	3
2 edge	u s s	s u s	s s s	s s s	0	0	1	1	0	0	0	1	0	0	1	1	19	0	1	3	3
2 edge	d s s	s s d	s s s	s s s	0	0	1	1	0	0	0	1	0	1	0	0	20	0	2	3	3
2 edge	d s s	s s u	s s s	s s s	0	0	1	1	0	0	0	1	0	1	0	1	21	0	2	3	3
2 edge	u s s	s s d	s s s	s s s	0	0	1	1	0	0	0	1	0	1	1	0	22	0	2	3	3
2 edge	u s s	s s i	s s s	s s s	0	0	1	1	0	0	0	1	0	1	1	1	23	0	2	3	3
2 edge	d s s	s s s	d s s	s s s	0	0	1	1	0	0	0	1	1	0	0	0	24	0	3	0	3
2 edge	d s s	s s s	u s s	s s s	0	0	1	1	0	0	0	1	1	0	0	1	25	0	3	0	3
2 edge	u s s	s s s	d s s	s s s	0	0	1	1	0	0	0	1	1	0	1	0	26	0	3	0	3

| | | |

FIG. 6 (cont.)

| | | |



| | | |

| | | |

3edge	s	u	s	s	d	s	s	u	s	s	s	s	0	0	1	1	1	1	0	0	0	1	0	1	197	1	1	1	3
3edge	s	u	s	s	u	s	s	d	s	s	s	s	0	0	1	1	1	1	0	0	0	1	1	0	198	1	1	1	3
3edge	s	u	s	s	u	s	s	u	s	s	s	s	0	0	1	1	1	1	0	0	0	1	1	1	199	1	1	1	3
3edge	s	d	s	s	d	s	s	s	d	s	s	s	0	0	1	1	1	1	0	0	1	0	0	0	200	1	1	2	3
3edge	s	d	s	s	d	s	s	s	u	s	s	s	0	0	1	1	1	1	0	0	1	0	0	1	201	1	1	2	3
3edge	s	d	s	s	u	s	s	s	d	s	s	s	0	0	1	1	1	1	0	0	1	0	1	0	202	1	1	2	3
3edge	s	d	s	s	u	s	s	s	u	s	s	s	0	0	1	1	1	1	0	0	1	0	1	1	203	1	1	2	3
3edge	s	u	s	s	d	s	s	s	d	s	s	s	0	0	1	1	1	1	0	0	1	1	0	0	204	1	1	2	3
3edge	s	u	s	s	d	s	s	s	u	s	s	s	0	0	1	1	1	1	0	0	1	1	0	1	205	1	1	2	3
3edge	s	u	s	s	u	s	s	s	d	s	s	s	0	0	1	1	1	1	0	0	1	1	1	0	206	1	1	2	3
3edge	s	u	s	s	u	s	s	s	u	s	s	s	0	0	1	1	1	1	0	0	1	1	1	1	207	1	1	2	3
3edge	s	d	s	s	d	s	s	s	s	d	s	s	0	0	1	1	1	0	1	0	0	0	0	0	208	1	1	3	0
3edge	s	d	s	s	d	s	s	s	s	u	s	s	0	0	1	1	1	0	1	0	0	0	0	1	209	1	1	3	0
3edge	s	d	s	s	u	s	s	s	s	d	s	s	0	0	1	1	1	0	1	0	0	1	0	0	210	1	1	3	0
3edge	s	d	s	s	u	s	s	s	s	u	s	s	0	0	1	1	1	0	1	0	0	1	1	1	211	1	1	3	0
3edge	s	u	s	s	d	s	s	s	s	d	s	s	0	0	1	1	1	0	1	0	1	0	0	0	212	1	1	3	0
3edge	s	u	s	s	d	s	s	s	s	u	s	s	0	0	1	1	1	0	1	0	1	0	0	1	213	1	1	3	0
3edge	s	u	s	s	u	s	s	s	s	d	s	s	0	0	1	1	1	0	1	0	1	1	0	0	214	1	1	3	0
3edge	s	u	s	s	u	s	s	s	s	u	s	s	0	0	1	1	1	0	1	0	1	1	1	1	215	1	1	3	0
3edge	s	d	s	s	s	d	s	s	d	s	s	s	0	0	1	1	1	0	1	1	0	0	0	0	216	1	2	2	3
3edge	s	d	s	s	s	d	s	s	u	s	s	s	0	0	1	1	1	0	1	1	0	0	1	1	217	1	2	2	3
3edge	s	d	s	s	s	u	s	s	d	s	s	s	0	0	1	1	1	0	1	1	0	1	0	0	218	1	2	2	3
3edge	s	d	s	s	s	u	s	s	u	s	s	s	0	0	1	1	1	0	1	1	0	1	1	1	219	1	2	2	3
3edge	s	u	s	s	s	d	s	s	d	s	s	s	0	0	1	1	1	0	1	1	1	0	0	0	220	1	2	2	3
3edge	s	u	s	s	s	d	s	s	u	s	s	s	0	0	1	1	1	0	1	1	1	0	1	1	221	1	2	2	3
3edge	s	u	s	s	s	u	s	s	d	s	s	s	0	0	1	1	1	0	1	1	1	1	0	0	222	1	2	2	3
3edge	s	u	s	s	s	u	s	s	u	s	s	s	0	0	1	1	1	0	1	1	1	1	1	1	223	1	2	2	3
3edge	s	d	s	s	s	d	s	s	s	d	s	s	0	0	1	1	1	1	0	0	0	0	0	0	224	1	2	3	0
3edge	s	d	s	s	s	d	s	s	s	u	s	s	0	0	1	1	1	1	0	0	0	0	0	1	225	1	2	3	0
3edge	s	d	s	s	s	u	s	s	s	d	s	s	0	0	1	1	1	1	0	0	0	1	0	0	226	1	2	3	0
3edge	s	d	s	s	s	u	s	s	s	u	s	s	0	0	1	1	1	1	0	0	0	1	1	1	227	1	2	3	0
3edge	s	u	s	s	s	d	s	s	s	d	s	s	0	0	1	1	1	1	0	0	1	0	0	0	228	1	2	3	0
3edge	s	u	s	s	s	d	s	s	s	u	s	s	0	0	1	1	1	1	0	0	1	0	1	1	229	1	2	3	0
3edge	s	u	s	s	s	u	s	s	s	d	s	s	0	0	1	1	1	1	0	0	1	1	0	0	230	1	2	3	0

FIG. 6 (cont.)

| | | |

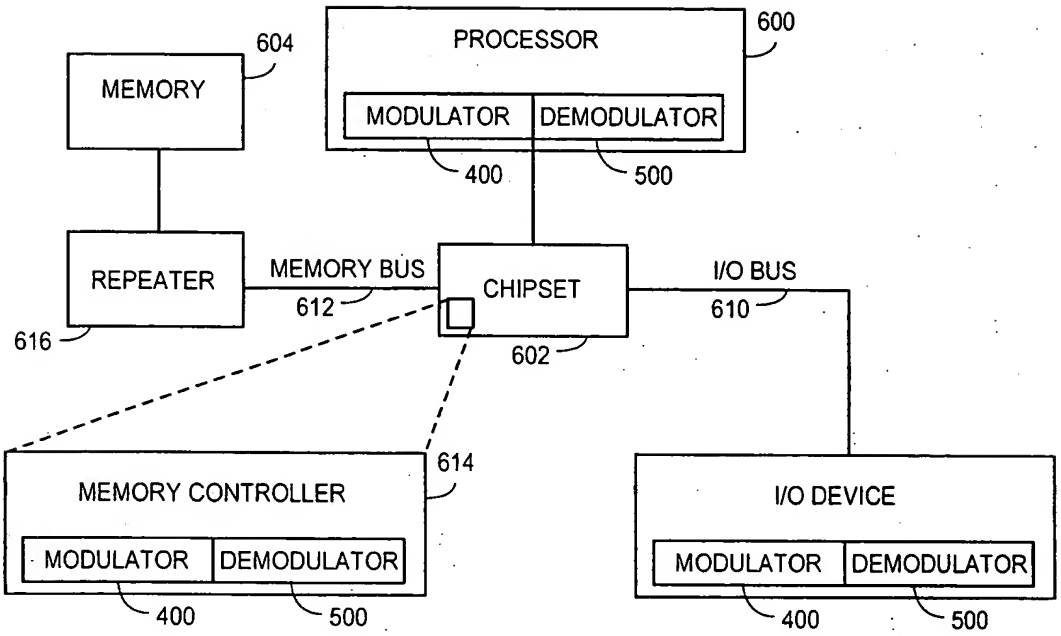

PROCESSOR
600
MODULATOR
DEMODULATOR
400
500
MEMORY
604
REPEATER
616
MEMORY BUS
612
CHIPSET
602
I/O BUS
610
MEMORY CONTROLLER
614
MODULATOR
DEMODULATOR
400
500
I/O DEVICE
MODULATOR
DEMODULATOR
400
500

FIG. 7